11. If any bit does not verify as programmed, repeat steps 2 through 9 until the bit has received a total of 1msec of programming time. Bits which do not program within 1msec are programming rejects. No further attempt to program these parts should be made.

12. Repeat steps 1 through 11 for all other bits to be programmed in the PROM.

13. Programming rejects returned to the factory must be accompanied by data giving address, desired data, and actual output data of the location in which a programming failure has occured.

Typical Programming Circuit

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand up to 11.0 volts during programming.

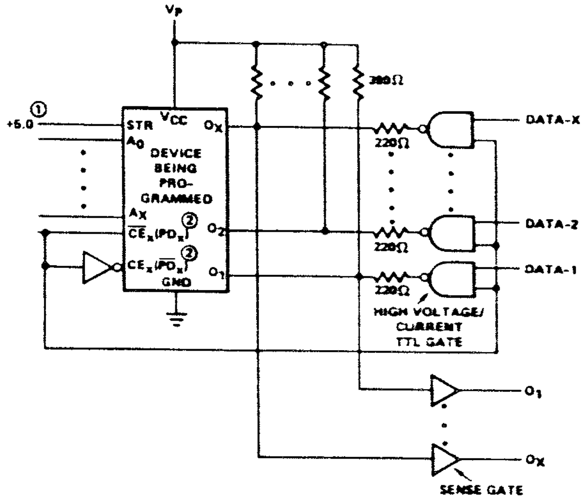


FIGURE 1

① The strobe input must remain at V_{IH} throughout the procedure. (for latched output devices only.)

② Disregard for devices with no enable inputs.

NOTE: For the 7629, pin 23 must remain at 5V during programming.

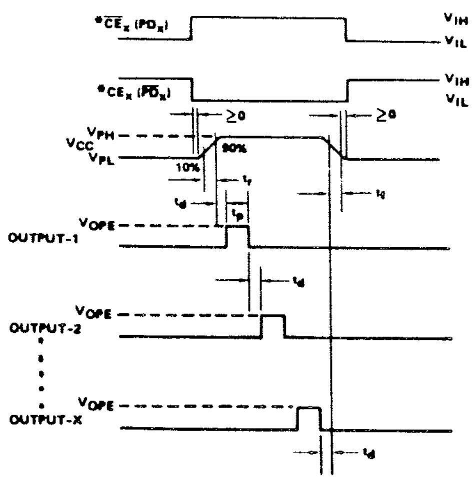


FIGURE 2

* Disregard for devices with no enable inputs.

The strobe input must remain at V_{IH} throughout the procedure. (for latched output devices only.)

This timing diagram shows device terminal conditions. Each positive going data pulse at the terminal blows the corresponding bit, resulting in a low output for that bit. Therefore, a low input at the DATA-X points of the Figure 1 circuit results in a permanent low output of a bit.

2

256-BIT BIPOLAR PROM (32X8) — 82S23 (O.C.)/82S123 (T.S.)

82S23-F,N • 82S123-F,N

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S23 and 82S123 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S23 and 82S123 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S23/123, N or F, and for the military temperature range (-55°C to +125°C) specify S82S23/123, F only.

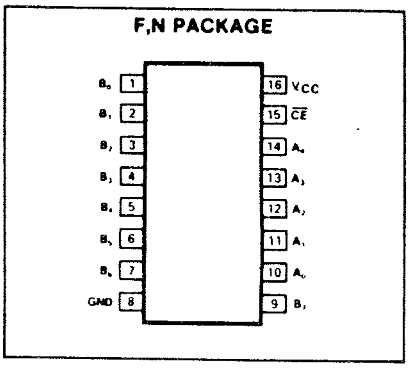
FEATURES

- **Address access time:**
  - **N82S23/123: 50ns max**
  - **S82S23/123: 65ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  - **N82S23/123: -100μA max**
  - **S82S23/123: -150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S23: Open collector**
  - **82S123: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

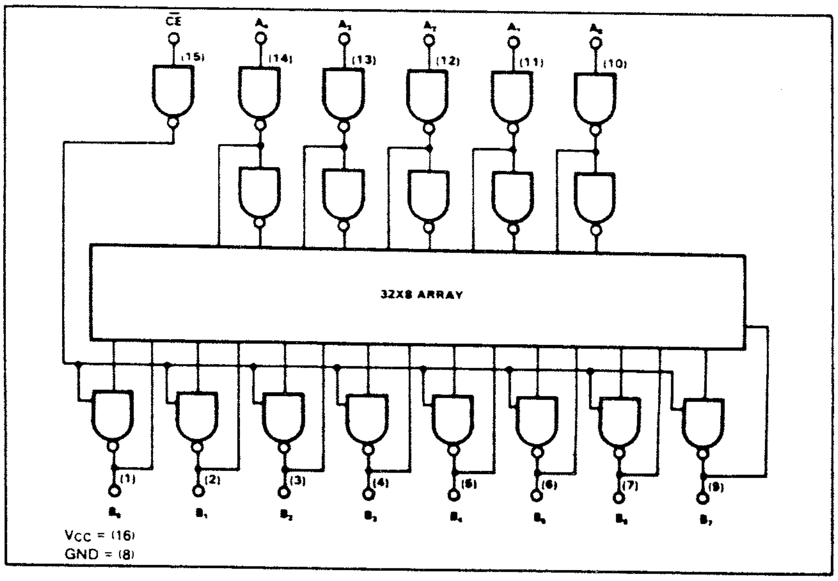
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
Vcc	Supply voltage	+7	Vdc
VIN	Input voltage	+5.5	Vdc
	Output voltage		Vdc
VOH	High (82S23)	+5.5	
VO	Off-state (82S123)	+5.5	
	Temperature range		°C
TA	Operating		
	N82S23/123	0 to +75	
	S82S23/123	-55 to +125	
TSTG	Storage	-65 to +150	

256-BIT BIPOLAR PROM (32X8) — 82S23 (O.C.)/82S123 (T.S.)

82S23-F,N • 82S123-F,N

DC ELECTRICAL CHARACTERISTICS

N82S23/123: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S23/123: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S23/123			S82S23/123			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				0.85			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								µA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			50			50	
	Output current								
I_{OLK}	Leakage (82S23)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			50	µA
$I_{O(OFF)}$	Hi-Z state (82S123)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			50	µA
		$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-50	
I_{OS}	Short circuit (82S123)	V_{OUT} = 0V	-20		-90	-20		-100	mA
I_{CC}	V_{CC} supply current			65	77		65	85	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

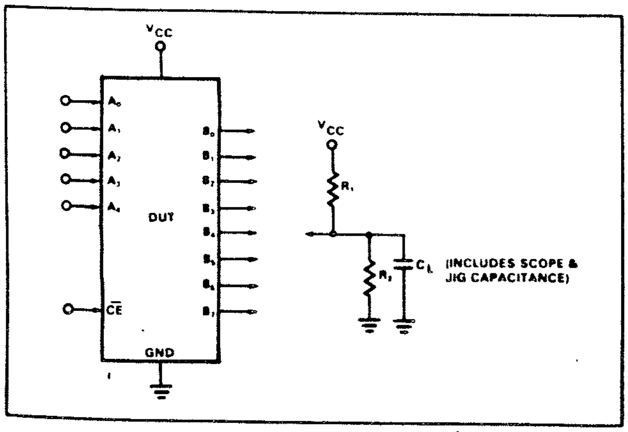
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$[1]
N82S23/123: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S23/123: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

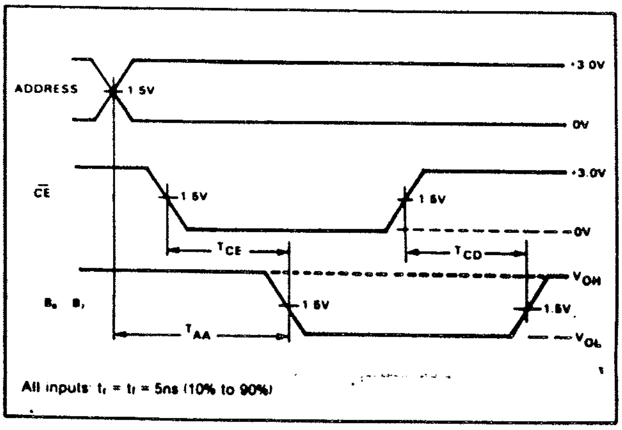
PARAMETER		TO	FROM	N82S23/123			S82S23/123			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{AA}[3]		Output	Address		35	50		35	65	
T_{CE}		Output	Chip enable		25	35		25	40	
	Disable time									ns
T_{CD}		Output	Chip disable		25	35		25	40	

NOTES
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.
3. Tested at an address cycle time of 1µsec

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS[4] $T_A = 25°C$. (Testing of these limits may cause programming of device.)

	PARAMETER	TEST CONDITIONS	LIMITS Min	Typ	Max	UNIT
V_{CCP}	Power supply voltage To program[1]	$I_{CCP} = 425 \pm 75mA$, Transient or steady state	8.5		9.0	V
	Verify limit					V
V_{CCVH}	Upper		5.3		5.7	
V_{CCVL}	Lower		4.3		4.7	
V_S	Verify threshold[2]		1.4		1.6	V
I_{CCP}	Programming supply current	$V_{CCP} = +8.75 \pm .25V$	350		500	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0		0.8	
	Input current					µA
I_{IH}	High	$V_{IH} = +5.5V$			50	
I_{IL}	Low	$V_{IL} = +0.4V$			-500	
V_{OPF}	Forced output voltage (program)[3]	$I_{OPF} = 200 \pm 20mA$, Transient or steady state	16.0		18.0	V
I_{OPF}	Forced output current (program)	$V_{OPF} = +17 \pm 1V$	180		220	mA
T_R	Output pulse rise time		10			µs
t_P	$\overline{CE}$ programming pulse width		100		125	µs
t_D	Pulse sequence delay		5			µs
t_V	$\overline{CE}$ verify pulse width		1			µs
T_{PVA}	Address program-verify cycle				1	ms
T_{PVM}	Memory program-verify time (continuous)				20	sec
F_L	Fusing attempts per link				1	cycle

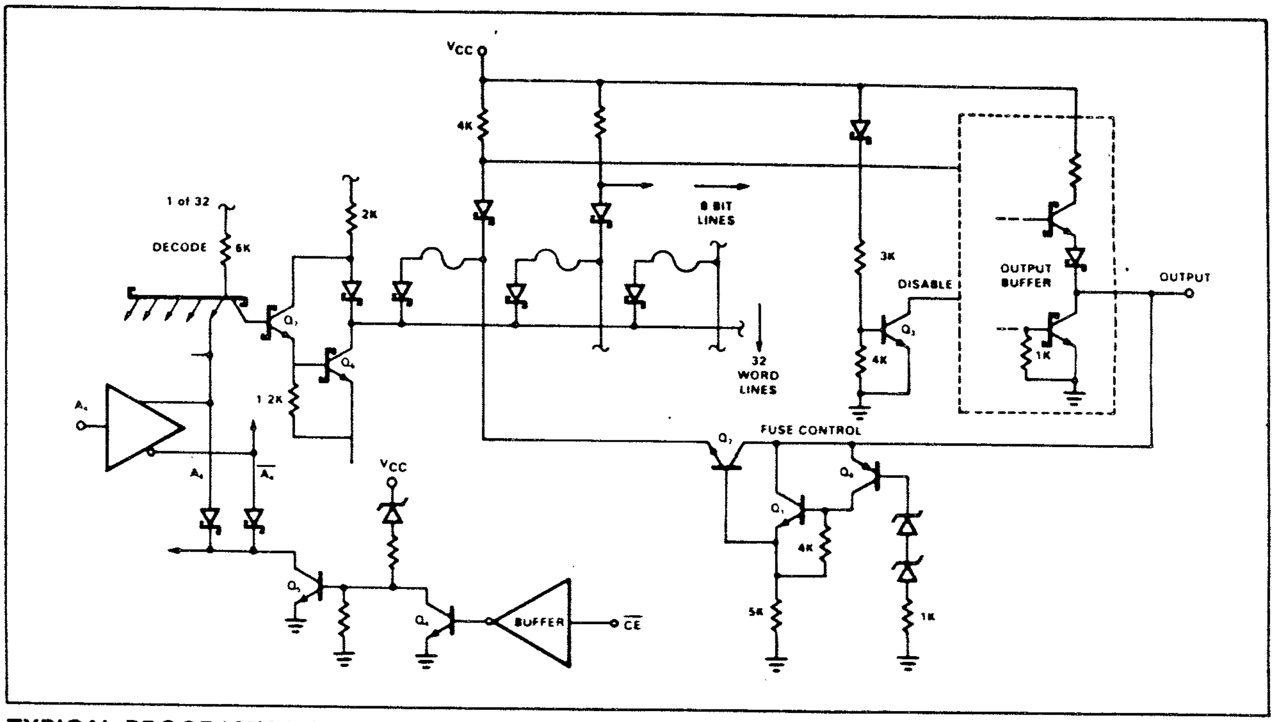
PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of 2V/µs, and 10µs maximum recovery
4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede but do not obsolete the performance requirements of previously manufactured programming equipment.

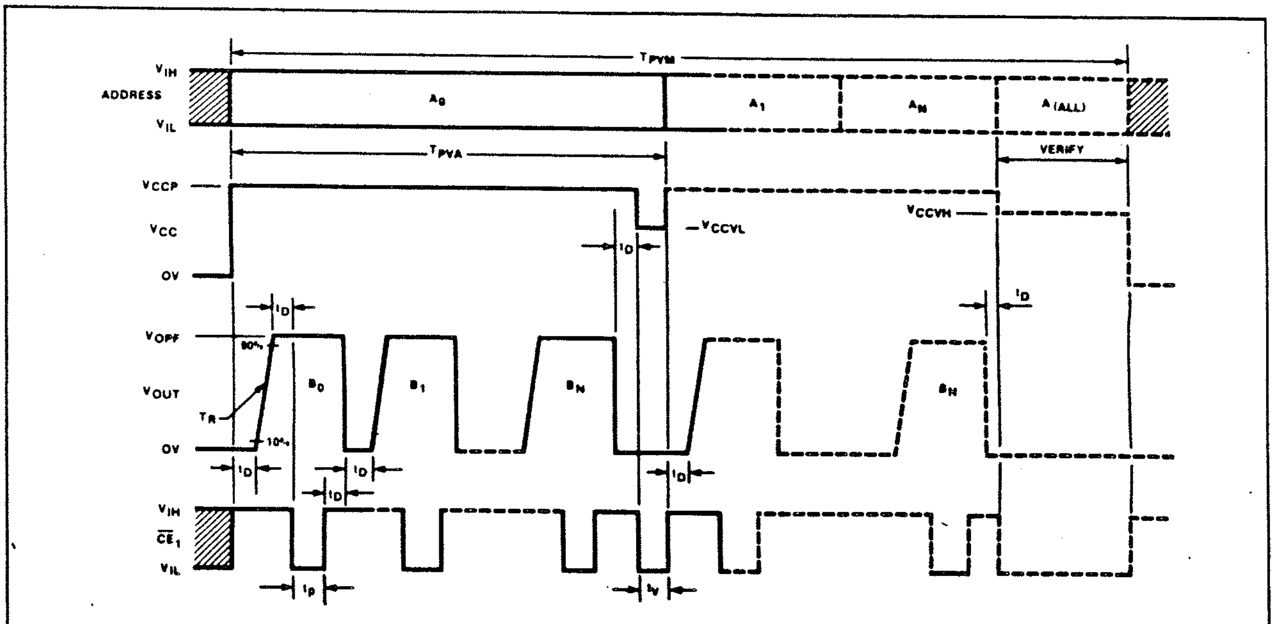
PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP}.
3. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time.
4. After t_D delay, pulse the $\overline{CE}$ input to logic low for a time t_P.
5. After t_D delay, remove V_{OPF} from the programmed output.
6. Repeat steps 3 through 5 to program other bits at the same address.
7. To verify programming of all bits at the same address after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the $\overline{CE}$ input. All programmed outputs should remain in the logic high state.
8. After t_D delay, repeat steps 2 through 7 to program and verify all other address locations.
9. After t_D delay raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to $\overline{CE}$, and cycling through all device addresses.

TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low Vcc margins is optional. For convenience, verification can also be executed at the operating Vcc limits specified in the dc characteristics

PROGRAMMABLE ARRAY LOGIC

Programming Features: PROMs (NiCr)

Programming Procedure

1. Apply the desired address to the inputs.
2. Enable Inputs may be left at any state.*
3. Apply 5.5 V to V_{CC}.
4. Apply V_{PP} to the program pin. (This step is not used on the 32 x 8 PROM).*
5. Apply V_{OUT} to the output to be programmed (Program only one output at a time).
6. Remove V_{OUT}.
7. Remove V_{PP}.
8. Verification may be performed after each bit or word or after completing the programming of all memory locations.

*The 5330/1 and 6330/1 do not have a program pin. For these devices the output only is used in programming a particular selected bit and the device must be in the disabled state.

Optimized Programming Algorithm

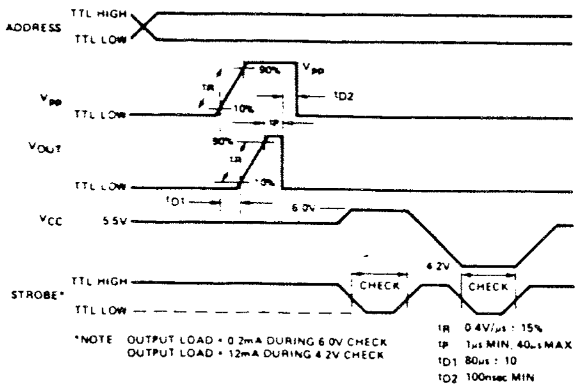
1. Pulse all fuses to be programmed with single, minimum voltage programming pulses (line 1 in the table).
2. Verify all fuses at low V_{CC} (4.2 V). During this step, unprogrammed fuses are pulsed up to eight more times (see table).
3. Re-verify at low V_{CC} (4.2 V) and high V_{CC} (6 V)

Pulse Number	Program Pin Voltage	Output Voltage
1 to 3	27 V	20 V
4 to 6	30 V	23 V
7 to 9	33 V	26 V

Verification Procedure

1. Enable the device.
2. To verify low-state:
   - 2A. Apply an address where the output should be low.
   - 2B. Apply 4.2 V to V_{CC}.
   - 2C. Load the output with I_{OL} = 12 mA.
   - 2D. Check that the output is less than 0.8 V.
3. To verify High-state:
   - 3A. Apply an address where the output should be high.
   - 3B. Apply 6 V to V_{CC}.
   - 3C. Load the output with I_{OH} = 0,3 mA.
   - 3D. Check that the output is higher than 4.5 V.

Programming Timing



Programming Parameters (Do not test these parameters or you will program the device)

Symbol	Parameter	Conditions T_A = +25 °C	Figure	Limits Min	Limits Typ	Limits Max	Unit
t_R	Slew rate of Programming Pulses +			0.3		0.5	V/μs
V_{CCP}	VCC during Programming			5.4	5.5	5.6	V
	Maximum Duty Cycle					25	%
V_{PP}	Programming Voltage on Program Pin*		1	27		33	V
V_{OUT}	Programming Voltage on Output Pin*		1	20		26	V
t_{D1}	Delay between Vpp and V_{OUT}		1	0	10	20	μs
t_{D2}				0	0.5	1	
t_p	Pulse Width of V_{OUT}		1	10		25	μs
V_{OLV}	V_{OL} during verification	Chip enabled I_{OL} = 12 mA V_{CC} = 4,2 V	2			0.8	V
V_{OHV}	V_{OH} during verification	Chip enabled I_{OH} = 0.3 mA V_{CC} = 6 V	2	4.5			V

+ Voltage supply must be capable of supplying at least 240 mA
* Leading edge of V_{PP} and V_{OUT}

PROGRAMMING

Programming Features: PROMs (TiW)

Programming Description

To program a particular bit normal TTL levels are applied to all inputs. Programming occurs when:

1. V_{CC} is raised to an elevated level.
2. The output to be programmed is raised to an elevated level.
3. The device is enabled.

In order to avoid misprogramming the PROM only one output at a time is to be programmed. Outputs not being programmed should be left open or connected to V_{CC} (4.2 V to 6.2 V) via 5K Ω resistors.

Programming Sequence

The sequence of programming conditions is critical and must occur in the following order:

1. Select the appropriate address with chip disabled.
2. Increase V_{CC} to programming voltage.
3. Increase appropriate output voltage to programming voltage.
4. Enable chip for programming pulse width.
5. Decrease V_{OUT} and V_{CC} to normal levels.

Programming Timing

In order to insure the proper sequence, a delay of 100 ns or greater must be allowed between steps. The enabling pulse must not occur less than 100 ns after the output voltage reaches programming level. The rise time of the voltage on VCC and the output must be between 1 and 10 V/μs.

Verification

After each programming pulse verification of the programmed bit should be made with both low and high V_{CC}. The loading of the output is not critical and any loading within the DC specifications of the part is satisfactory.

Additional Pulses

Up to 10 programming pulses should be applied until verification indicates that the bit has programmed. After verification an additional 5 programming pulses must be applied to insure the reliability of the programmed bit.

Programming Registered PROMs

The asynchronous registered PROM is programmed in the same manner as standard PROMs.
The synchronous registered PROM is programmed in similar fashion with one exception: the program enable is registered and therefore must be blocked.

Programming Waveforms

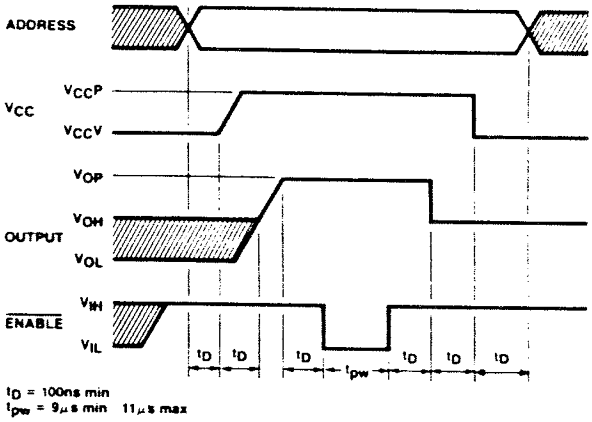


Figure 1

Note: Programming pulse t_{pw} is applied for 5 additional pulses after verification indicates a bit is blown.

Programming Parameters (Do not test these parameters or you may program the device)

Symbol	Parameter	Recommended Value			Unit
		Min	Typ	Max	
V_{CCP}	Required V_{CC} for programming	10.5	11.0	11.5	V
V_{OP}	Required output voltage for programming	10.5	11.0	11.5	V
t_R	Rise time of V_{CC} or V_{OUT}	1.0	5.0	10.0	V/μs
I_{CCP}	Current limit of V_{CCP} supply	800	1000	–	mA
I_{OP}	Current limit of V_{OP} supply	15	20	–	mA
t_{PW}	Programming pulse width (enabled)	9	10	11	μs
V_{CC}	Low V_{CC} for verification	4.2	4.3	4.4	V
V_{CC}	High V_{CC} for verification	5.8	6.0	6.2	V
MDC	Maximum duty cycle of V_{CCP}	–	25	25	%
t_D	Delay time between programming steps	100	120	–	ns
V_{IL}	Input low level	0	0	0.5	V
V_{IH}	Input high level	2.4	3.0	5.5	V