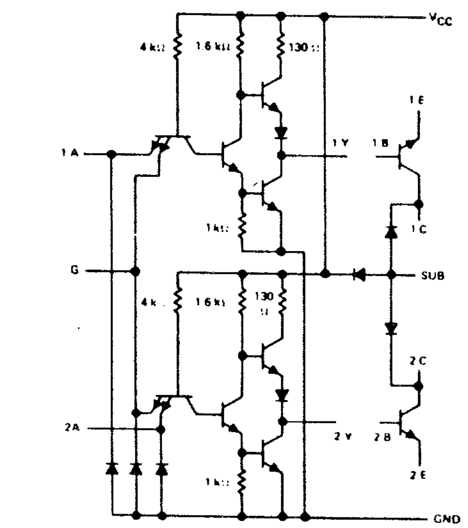
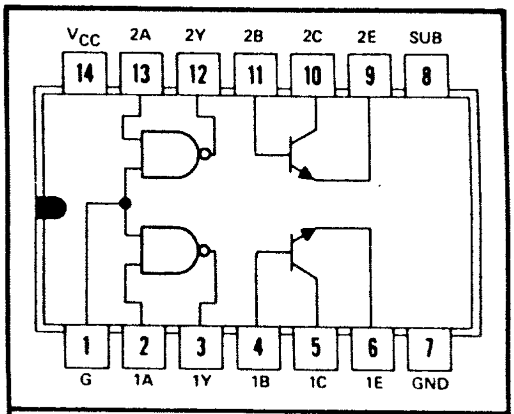
TYPES SN55460, SN75460
DUAL PERIPHERAL POSITIVE-AND DRIVERS

schematic



Resistor values shown are nominal

SN55460 . . . J
SN75460 . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = $\overline{AG}$ (gate only)
C = AG (gate and transistor)

4

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER		TEST CONDITIONS†	SN55460			SN75460			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.8			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		2.4	3.3		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.25	0.5		0.25	0.4	V
I_I Input current at maximum input voltage	input A	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
	input G				2			2	
I_{IH} High-level input current	input A	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
	input G				80			80	
I_{IL} Low-level input current	input A	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
	input G				−3.2			−3.2	
I_{OS} Short-circuit output current§		V_{CC} = MAX	−18	−35	−55	−18	−35	−55	mA
I_{CCH} Supply current, outputs high		V_{CC} = MAX, V_I = 0		2.8	4		2.8	4	mA
I_{CCL} Supply current, outputs low		V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values at V_{CC} = 5 V, T_A = 25 C.
§ Not more than one output should be shorted at a time.

TYPES SN55460, SN75460
DUAL PERIPHERAL POSITIVE-AND DRIVERS

4

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS†		SN55460 MIN	SN55460 TYP‡	SN55460 MAX	SN75460 MIN	SN75460 TYP‡	SN75460 MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0		40			40			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 10 mA, I_B = 0, See Note 8		25			25			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		40			40			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 100 mA, T_A = 25 C	See Note 8	25			25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25 C		30			30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = MIN		10			20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = MIN		15			25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA, I_C = 100 mA	See Note 8		0.85	1.2		0.85	1	V
		I_B = 30 mA, I_C = 300 mA			1	1.4		1	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA, I_C = 100 mA	See Note 8		0.25	0.5		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA			0.45	0.8		0.45	0.7	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 8: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Figure 1		22		ns
t_{PHL}	Propagation delay time, high-to-low-level output			8		ns

output transistors

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_d	Delay time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω, See Figure 2		10		ns
t_r	Rise time			16		ns
t_s	Storage time			23		ns
t_f	Fall time			14		ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor paramters.

gates and transistors combined

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_C ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	50	ns
t_{TLH}	Transition time, low-to-high-level output			10	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, I_C ≈ 300 mA, R_{BE} = 500 Ω, See Figure 4	V_S−10			mV

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

National Semiconductor

Digital-to-Analog Converters

DAC0808, DAC0807 DAC0806 8-Bit D/A Converters

DAC0808, DAC0807, DAC0806

3

general description

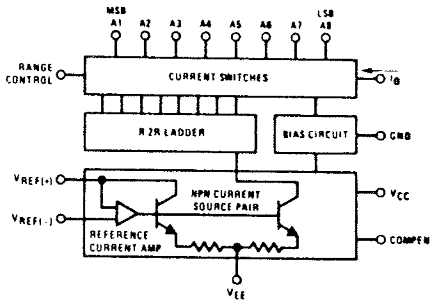
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

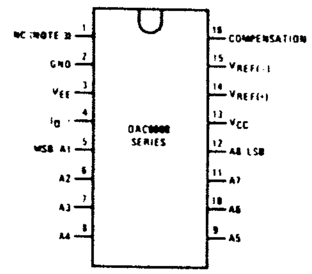
features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

block and connection diagrams

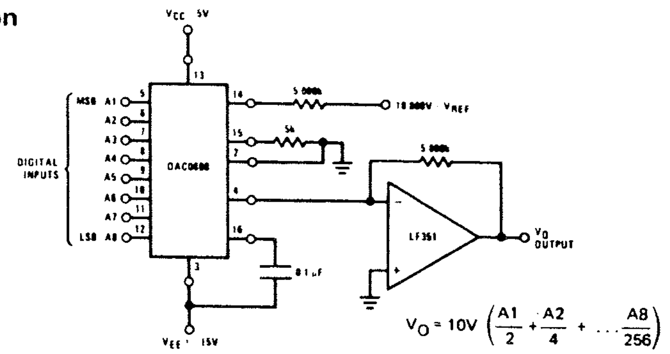


Dual-In-Line Package



TOP VIEW

typical application



$$V_O = 10V\left(\frac{A1}{2} + \frac{A2}{4} + \dots \frac{A8}{256}\right)$$

FIGURE 1. ±10V Output Digital to Analog Converter

ordering information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS*					
		D PACKAGE (D16C)		J PACKAGE (J16A)		N PACKAGE (N16A)	
8-bit	−55°C ≤ T_A ≤ +125°C	DAC0808LD	LM1508D-8	DAC0808LJ	LM1508J-8		
8-bit	0°C ≤ T_A ≤ +75°C			DAC0808LCJ	LM1408J-8	DAC0808LCN	LM1408N-8
7-bit	0°C ≤ T_A ≤ +75°C			DAC0807LCJ	LM1408J-7	DAC0807LCN	LM1408N-7
6-bit	0°C ≤ T_A ≤ +75°C			DAC0806LCJ	LM1408J-6	DAC0806LCN	LM1408N-6

*Note. Devices may be ordered by using either order number.

DAC0808, DAC0807, DAC0806

absolute maximum ratings (T_A = 25°C unless otherwise noted)

Power Supply Voltage	
V_{CC}	5.5 V_{DC}
V_{EE}	−16.5 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Package Limitation)	
Cavity Package	1000 mW
Derate above T_A = 25°C	6.7 mW/°C
Operating Temperature Range	
DAC0808L	$-55°C \leq T_A \leq +125°C$
DAC0808LC Series	$0 \leq T_A \leq +75°C$
Storage Temperature Range	−65°C to +150°C

electrical characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808L: T_A = −55°C to +125°C, DAC0808LC, DAC0807LC, DAC0806LC, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

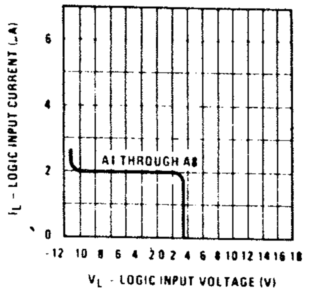
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
	DAC0808L (LM1508-8), DAC0808LC (LM1408-8)				±0.19	%
	DAC0807LC (LM1408-7), (Note 1)				±0.39	%
	DAC0806LC (LM1408-6), (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	T_A = 25°C (Note 2), *(Figure 5)*		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 3)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 3)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−5	μA
	Output Current Range	*(Figure 3)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω, *(Figure 3)*	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 3)*		0	4	μA
	Output Voltage Compliance Pin 1 Grounded,	$E_r \leq 0.19\%$, T_A = 25°C			−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}
$SR I_{REF}$	Reference Current Slew Rate	*(Figure 6)*		8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \leq V_{EE} \leq -16.5V$		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	*(Figure 3)*				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

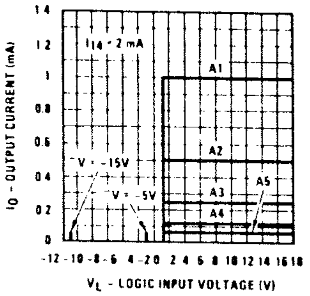
typical performance characteristics

V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

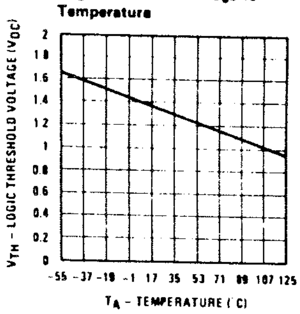
Logic Input Current vs Input Voltage



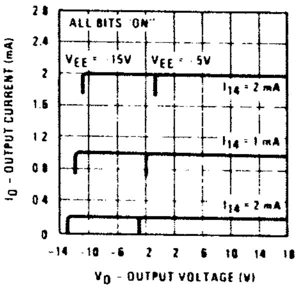
Bit Transfer Characteristics



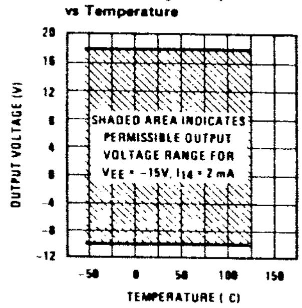
Logic Threshold Voltage vs Temperature



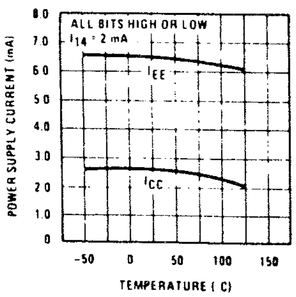
Output Current vs Output Voltage (Output Voltage Compliance)



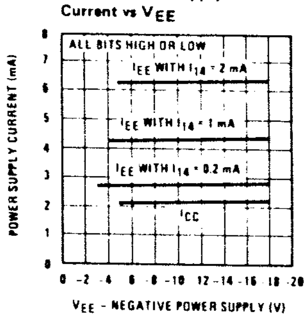
Output Voltage Compliance vs Temperature



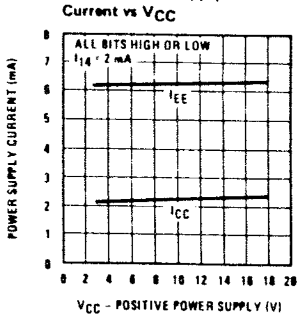
Typical Power Supply Current vs Temperature



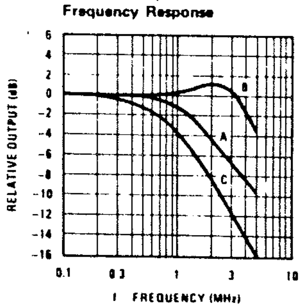
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 9* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

DAC0808, DAC0807, DAC0806

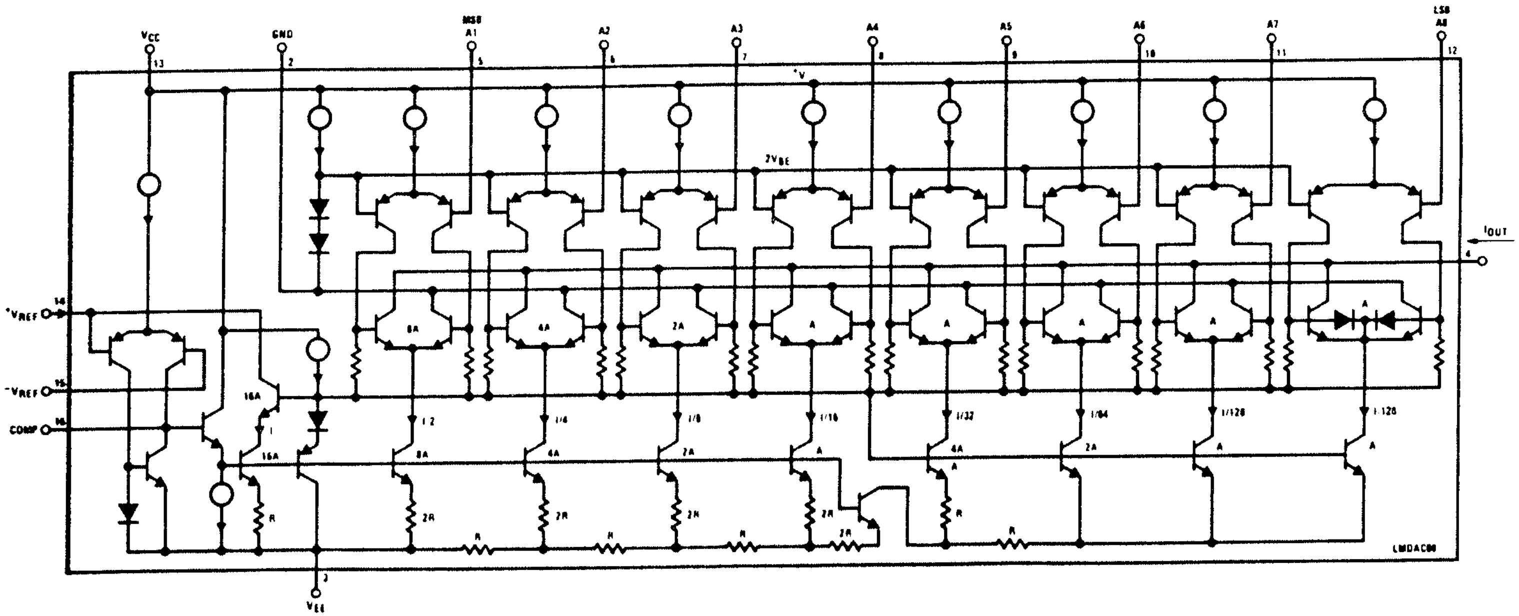
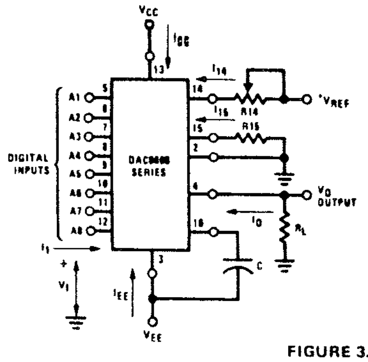


FIGURE 2 Equivalent Circuit of the DAC0808 Series

test circuits



V_I and I_I apply to inputs A1–A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

where $K \cong \dfrac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level

A_N = "0" if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit

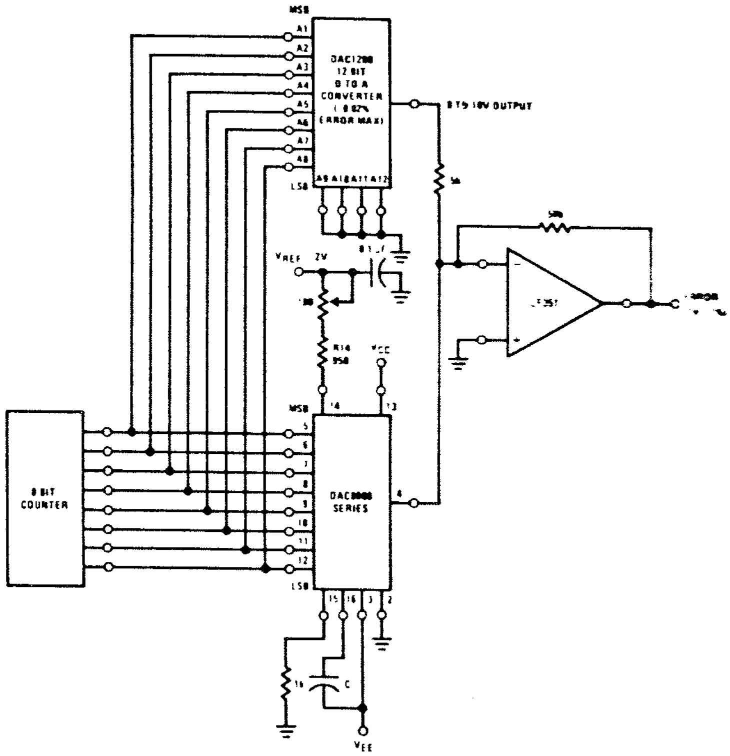


FIGURE 4. Relative Accuracy Test Circuit

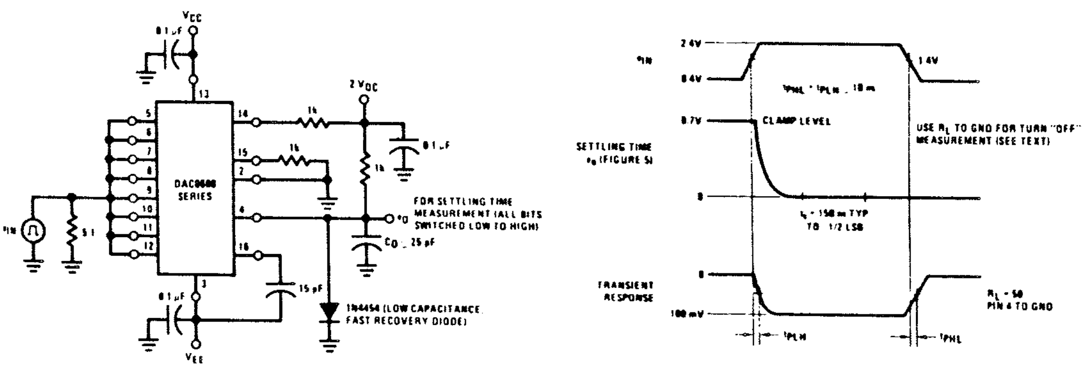


FIGURE 5. Transient Response and Settling Time

test circuits (Continued)

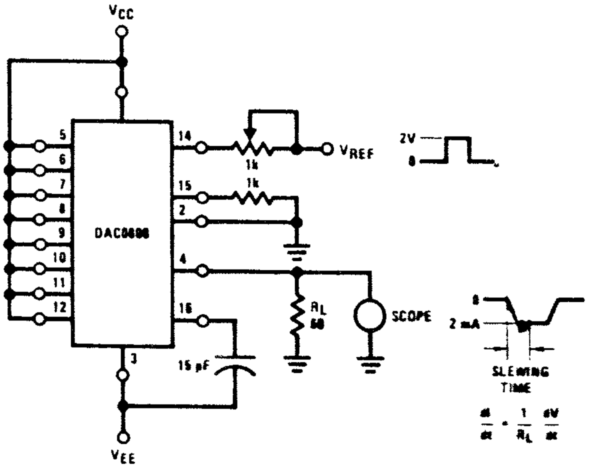


FIGURE 6. Reference Current Slew Rate Measurement

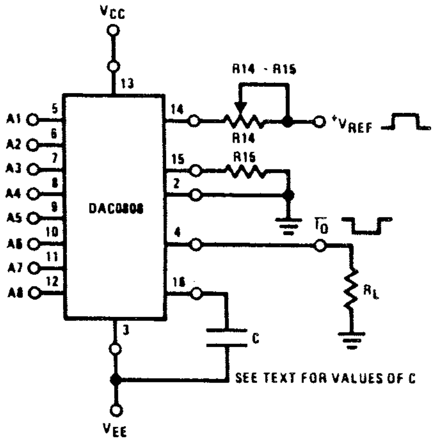


FIGURE 7. Positive V_{REF}

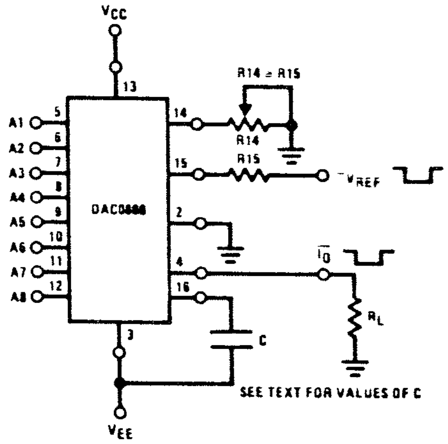


FIGURE 8. Negative V_{REF}

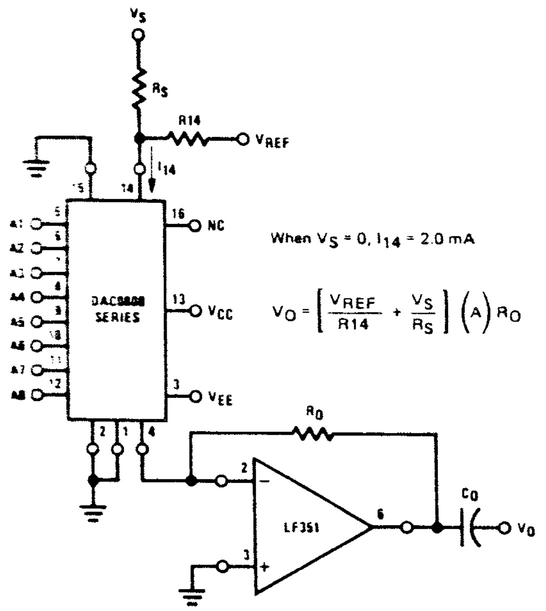


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit

application hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 kΩ, minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

application hints (Continued)

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to 0.5V when V_{EE} = −5V due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to −5V where the negative supply voltage is more negative than −10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 kΩ between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance, but a 2.5 kΩ load increases worst-case settling time to 1.2 μs (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than −7V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within ±1/2 LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in *Figure 4*. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μA to 4 mA, the additional error contributions are less than 1.6 μA. This is well within 8-bit accuracy when referred to full-scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

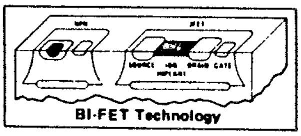
SETTLING TIME

The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 100 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25$ pF.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactoy test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

National Semiconductor

Amplifiers



LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

LF155, LF155A, LF255, LF355, LF355A, LF355B low supply current
LF156, LF156A, LF256, LF356, LF356A, LF356B wide band
LF157, LF157A, LF257, LF357, LF357A, LF357B wide band decompensated (AV_{MIN} = 5)

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

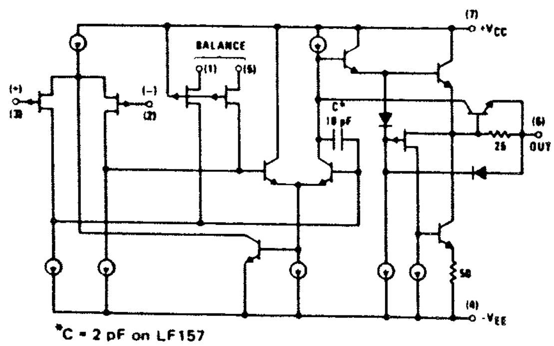
(LF155A, LF156A, LF157A)

Low input bias current	30 pA
Low input offset current	3 pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1 mV
Low input offset voltage temperature drift	$3\mu V/^{\circ}C$
Low input noise current	$0.01\ pA/\sqrt{Hz}$
High common-mode rejection ratio	100 dB
Large dc voltage gain	106 dB

Uncommon Features

	LF155A	LF156A	LF157A (A_V = 5)*	UNITS
Extremely fast settling time to 0.01%	4	1.5	1.5	μs
Fast slew rate	5	12	50	$V/\mu s$
Wide gain bandwidth	2.5	5	20	MHz
Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

Simplified Schematic



*C = 2 pF on LF157

LF155/LF156/LF157 Series

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